ERROR CORRECTING MEMORY AND METHOD OF OPERATING SAME

Wingyu Leung
Fu-Chieh Hsu

ABSTRACT

A memory device that uses error correction code (ECC) circuitry to improve the reliability of the memory device in view of single-bit errors caused by hard failure or soft error. A write buffer is used to post write data, so that ECC generation and memory write array operation can be carried out in parallel. As a result there is no penalty in write latency or memory cycle time due to ECC generation. A write-back buffer is used to post corrected ECC words during read operations, so that write-back of corrected ECC words does not need to take place during the same cycle that data is read. Instead, write-back operations are performed during idle cycles when no external memory access is requested, such that the write back operation does not impose a penalty on memory cycle time or affect memory access latency.